REMARKS

The above amendments and following remarks are fully and completely responsive to the Office Action dated February 8, 2005. Claims 1, 3-8 and 10-14 are pending in this application with claims 1, 5-8, 10 and 11 amended by the present Amendment. In the outstanding Office Action, claims 1, 3, 5, 6, 8, 11 and 12 were rejected under 35 U.S.C. § 102(e); claims 4, 7 and 10 were rejected under 35 U.S.C. § 103(a) (two separate rejections); and claims 13 and 14 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. No new matter has been added. Claims 1, 3-8 and 10-14 are presented for reconsideration.

35 U.S.C. § 102(e)

Claims 1, 3, 5, 6, 8, 11 and 12 were rejected under 35 U.S.C. § 102(e) as being anticipated by Kraus et al. (U.S. Patent No. 6,587,979, "Kraus"). In making this rejection, the Office Action asserts that this reference teaches each element of the claimed invention. Applicants respectfully traverse this rejection.

Claim 1, as amended, recites in part:

> ...a built out self test (BOST) device which is coupled between the external test unit and the semiconductor device, wherein first pattern data for a pattern dependency test is previously stored in the BIST circuit and second pattern data for a timing dependency test is previously stored in the BOST device, wherein the BOST device includes
>
> a pattern generating circuit, coupled to the semiconductor device, for providing the previously stored second pattern data for the timing dependency test to the semiconductor device, and

> a decision circuit, coupled to the pattern generating circuit and the semiconductor device, for receiving test data originating from the second pattern data from the semiconductor device and determining the test result of the timing dependency test using the test data and the second pattern data.

In contrast, Kraus discloses that the BOST controller 71 executes a test program written into RAM 70 or stored in a ROM that replaces RAM 70. However, Kraus does not disclose 1) a pattern generating circuit for providing previously stored second pattern data for a timing dependency test to a semiconductor device, and 2) a decision circuit for receiving test data originating from the second pattern data from the semiconductor device and determining the test result of the timing dependency test using the test data and the second pattern data, as recited in claim 1. Specifically, Kraus states:

> The program stored in RAM 70 tells BOST controller 71 to carry out all test functions that might otherwise be carried out by tester 21 of Fig. 5 including supplying test pattern inputs to logic circuits 14, 16 via the I/O terminals of the IC 10, supplying control signal patterns to core wrappers 24 and glue logic circuit 36 via the RC, SCAN and JTAG buses, and appropriately processing IC output data appearing on the I/O and SCAN buses.

Column 15, lines 1-8.

As discussed above, the BOST controller 71 disclosed in Kraus requires a program stored either in RAM 70 or in a ROM to tell the BOST controller 71 how to function.

The BOST device of the present invention does not require a program to tell it how to operate.

The BOST device of the present invention includes the pattern generating circuit and the decision circuit. Accordingly, without having a test program, the pattern generating circuit provides the previously stored second pattern data for the timing dependency test to the semiconductor device and the decision circuit determines the test result of the timing dependency test using the test data from the semiconductor device and the second pattern data for the timing dependency test. Furthermore, the BIST circuit performs a pattern dependency test using the previously stored first pattern data for a pattern dependency test without having the test program.

Therefore, Kraus fails to teach and/or suggest the claimed invention. Specifically, this reference fails to teach and/or suggest a pattern generating circuit, coupled to the semiconductor device, for providing the previously stored second pattern data for the timing dependency test to the semiconductor device. This reference also fails to teach and/or suggest a decision circuit, coupled to the pattern generating circuit and the semiconductor device, for receiving test data originating from the second pattern data from the semiconductor device and determining the test result of the timing dependency test using the test data and the second pattern data. Therefore, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 1, 3, 5, 6, 8, 11 and 12 under 35 U.S.C. § 102(e).

35 U.S.C. § 103(a)

Claim 10 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Kraus. In making this rejection, the Office Action asserts that this reference teaches each element of the claimed invention. Applicants respectfully traverse this rejection.

Claim 10 has been amended to depend from independent claim 1, which is clearly distinguished from Kraus as discussed above. Accordingly, Applicants request reconsideration and withdrawal of the rejection of claim 10.

Claims 4 and 7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kraus in view of Leas et al. (U.S. Patent No. 5,600,257, "Leas"). The Office Action admits that Kraus fails to teach and/or suggest "the external tester unit provides the BOST device with an output level generating voltage" as recited in claim 4 and "a switch circuit for disconnecting the BIST controller 8 (BOST device) from the BIST circuit 7 (semiconductor device)" as recited in claim 7. Leas is cited for correcting these deficiencies in Kraus.

Leas, however, is not cited for, nor does Leas teach, a pattern generating circuit, coupled to the semiconductor device, for providing the previously stored second pattern data for the timing dependency test to the semiconductor device. Similarly, Leas is not cited for, nor does Leas teach, a decision circuit, coupled to the pattern generating circuit and the semiconductor device, for receiving test data originating from the second pattern data from the semiconductor device and determining the test result of the timing dependency test using the test data and second pattern data.

Accordingly, the combination of Leas and Kraus fails to teach and/or suggest the claimed invention. Therefore, Applicants request reconsideration and withdrawal of the rejection of claims 4 and 7 under 35 U.S.C. § 103(a).

Claim Objections

Claims 13 and 14 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. These claims depend indirectly from claim 1. As discussed above, claim 1 is allowable. Therefore, Applicants request reconsideration and withdrawal of the objection to claims 13 and 14.

Conclusion

Applicants' amendments and remarks have overcome the objection and rejections set forth in the Office Action dated February 8, 2005. Specifically, Applicants' remarks have distinguished claims 1, 3, 5, 6, 8, 11 and 12 from Kraus and thus overcome the rejection of these claims under 35 U.S.C. § 102(e). Applicants' remarks have also distinguished claim 10 from Kraus and thus overcome the rejection of this claim under 35 U.S.C. § 103(a). Furthermore, Applicants' remarks have distinguished claims 4 and 7 from the combination of Kraus and Leas and thus overcome the rejection of these claims under 35 U.S.C. § 103(a). Claims 13 and 14 were indicated as containing allowable subject matter, but were objected to as being dependent upon a rejected base claim. Applicants' remarks have distinguished the base claim from the cited prior art, thus overcoming the objection to claims 13 and 14. Accordingly, claims 1, 3-8 and 10-14 are in condition for allowance. Therefore, Applicants respectfully request consideration and allowance of claims 1, 3-8 and 10-14.

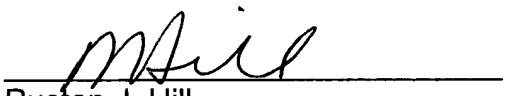
Applicants submit that the application is now in condition for allowance. If the Examiner believes the application is not in condition for allowance, Applicants respectfully

request that the Examiner contact the undersigned attorney by telephone if it is believed that such contact will expedite the prosecution of the application.

In the event that this paper is not considered to be timely filed, Applicants respectfully petition for an appropriate extension of time.

The Commissioner is authorized to charge payment for any additional fees which may be required with respect to this paper to our Deposit Account No. 01-2300, making reference to attorney docket number 108075-00075.

Respectfully submitted,
ARENT FOX PLLC



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